



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/621,449

07/18/2003

Nobuo Matsui

240541US2DIV

1115

22850

7590

08/24/2006

C. IRVIN MCCLELLAND
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER

ROSSOSHEK, YELENA

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/621,449

Applicant(s)

MATSUI ET AL.

Examiner

Helen Rossoshek

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/865,289.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. This office action is in response to the Application 10/621,449 filed 07/18/2003 and amendment filed 06/06/2006.

2. Claims 1-11 remain pending in the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/26/2006 has been entered.

4. Applicant's arguments have been fully considered and are persuasive. A new ground(s) of rejection is made.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Killian et al. (US Patent 7,020,854).

With respect to claims 1 and 6 Killian et al. teaches a processor (col. 1, ll.15-20), a system LSI (col. 32, ll.40-50); comprising: a processor core (as shown on the Fig. 2 core processor 60 (col. 10, ll.31-39)); and a memory operatively coupled to said processor (as shown on the Fig. 6, wherein core processor 60 (Fig. 2)/CPLD 202 coupled to various memory (col. 32, ll.62-67; col. 33, ll.1-7)); wherein said processor is designed (col. 9, ll.45-50) using the method comprising: selecting a cache size (using configuration options such as selecting instruction/data cache size (col. 11, ll.63-64; col. 19, ll.40-47); selecting an instruction memory size (col. 11, ll.60-62; col. 12, ll.15-17; ll.61-64); selecting a data memory size (col. 43, ll.17-24); selecting at least one of a plurality of option instructions that are provided respectively in correspondence with machine instructions to be implemented within said processor core (col. 24, ll.56-60; col. 6, ll.65-67; col. 29, ll.50-54).

With respect to claim 10 Killian et al. teaches a method of generating a design of a system LSI using a description language (abstract; col., 64-66), comprising: preparing a configuration specifying a file including variable item definition information concerning a multiprocessor configuration (using a configuration manager screen 86 to design configurable processor based on a base processor description (col. 45, ll.28-30) as shown on the Fig. 3 and having an ability to create a new file or edit an existing file (col. 11, ll.10-23), including configurable instruction set architecture (ISA), wherein variable are used to describe instructions (col. 16, ll.47-60; col. 7, ll.25-28)); creating a customized description language mode (within generating a customized synthesizable hardware description of the configurable processor (col. 10, ll.7-9)); and logically

Art Unit: 2825

composing said design based on said description language model, wherein said variable item definition information contains at least one item of option instruction information and information concerning a user defined module and a multiprocessor configuration (within generating a configurable process design based on the base processor description, a base instruction set (col. 45, ll.28-30) and a plurality of configurable features including additional instruction in the configuration specification, which is different from the base instructions (col. 45, ll.30-41), wherein variables are used in describing set of instructions (col. 16, ll.47-60).

With respect to claims 2-5, 7-9 and 11 Killian et al. teaches:

Claims 2 and 7: wherein said option instructions include a dividing option instruction (DIV) and a maximum/minimum value option instruction (MINMAX) (within "options" section menu shown on the display window of the Fig. 4, wherein configuration options are divided into plurality of options, for example "Implementation goals" (col. 11, ll.24-40), wherein each option instruction has minimum and maximum values such as "Target speed" from 100 MHz to 250 MHz (Fig. 4; col. 11, l.48; col. 19, ll.14-23);

Claims 3 and 8: wherein said processor core is provided with an instruction cache and a data cache (col. 11, ll.63-65);

Claims 4 and 9: wherein said cache size, said instruction memory size, said data memory size, and said option instructions are provided in RTL templates (col. 33, ll.9-11);

Claim 5: wherein said method further comprises selecting optional hardware associated with said processor (col. 17, ll.59-63);

Claim 11: wherein the description language comprises a hardware description language (HDL) (col. 7, ll.34-49).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Helen Rossoshek
AU 2825



A. M. Thompson
Primary Examiner
Technology Center 2800

